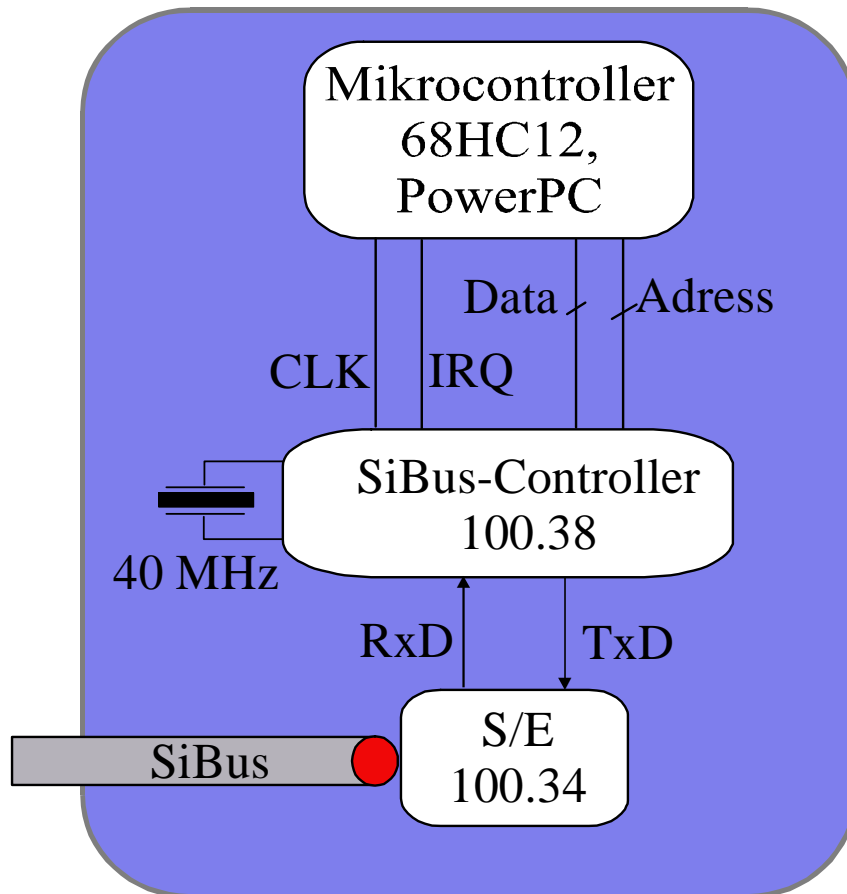


Overview



- * Bit rate : 10 Mbps
- * Programmable timing-registers to configure protocol wait times
- * Programmable bus master function
- * Double buffered receive storage scheme
- * 16 Message Buffer in total, 14 Byte wide each
- * Programmable Buffer Configuration (transmit, receive, FIFO)
- * Configurable CPU Interface to connect to 68HC12, Black-Oak PowerPC and 80C166
- * CPU access by locking mechanism
- * 10 maskable interrupt sources
- * Low power sleep mode

100.38: SiBus-Controller

Block-Diagram

